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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/571,426	03/10/2006	Mitsuyoshi Mori	071971-0494	3460
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EXAMINER				
NICTLY, JOSEPH C				
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

### Office Action Summary

**Application No.**

10/571,426

**Applicant(s)**

MORI ET AL.

**Examiner**

Joseph C. Nicely

**Art Unit**

2813

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 06 November 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) 2, 4 and 5 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1, 3, 6-12 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 10 March 2006 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SF/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

**FINAL ACTION**

1. This Office action is in response to the amendment filed 11/06/2008 in which claims 1, 3, and 6-8 were amended, claims 2 and 4-5 were cancelled, and claim 12 was added.
2. Claims 1, 3, and 6-12 are currently pending.

***Drawings***

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the subject matter of claim 8 (i.e., the last two elements which begin "during the step of implanting") must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner,

the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

***Claim Objections***

4. Claim 6 is objected to because of the following informalities: in line 3, "isolation" should read –silicon–. Appropriate correction is required.
5. Claim 7 is objected to because of the following informalities: in line 2, "isolation" should read –silicon–. Appropriate correction is required.

***Claim Rejections - 35 USC § 103***

6. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.
7. Examiner notes that a machine translation of JP 2004-039832 is used as an English language equivalent in the following rejections.
8. Claims 1, 3, 11, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshiko (JP 2004-039832 and Yoshiko hereinafter).

As to claim 1: Yoshiko discloses a **solid state imaging apparatus comprising: a photoelectric conversion section** (comprising at least 12, 18, and 19; [0096]) **formed in an imaging area of a silicon substrate, the photoelectric conversion section includes a surface layer (19) having a first conductivity type (p-type) provided on a top portion of the silicon substrate, a first semiconductor layer made of silicon (18) having a second conductivity type (n-type), and service as a charge accumulation region, provided under the surface layer** (Fig. 2; [0016]-[0021]; the phrase "service as a...region" is interpreted to be intended use and is thus given

little patentable weight); **and a second semiconductor layer made of silicon (12) having the first conductivity type (p-type) provided under the first semiconductor layer (Fig. 2; [0016]-[0021]); an isolation region (7b) formed in at least one part of the silicon substrate located around the photoelectric conversion section (comprising at least 12, 18, and 19) made of silicon material (Fig. 5(b); [0029]-[0030]) which fills an isolation trench formed on the semiconductor substrate (Fig. 5(a); [0029]-[0030]); a first silicon layer made of silicon (6) having the first conductivity type (p-type) formed in a region of the silicon substrate forming the bottom and sidewalls of the isolation trench (Fig. 5(a) and (b); [0029]); and a second silicon layer made of silicon (comprising 10 and 11) having the first conductivity type (p-type) in contact with a bottom side of the first silicon layer (Fig. 2; [0016]-[0021]), wherein the photoelectric conversion section (comprising 12, 18, and 19) is in contact with the isolation region (7b), the first silicon layer (6), and the second silicon layer (Fig. 2; second silicon layer comprising 10 and 11).**

Yoshiko fails to expressly disclose where **a depth of the isolation region is smaller than that of the first semiconductor layer**. Yoshiko discloses in [0024] the desirability of making the STI region small in width, but fails to expressly disclose the desired dimensions of the STI. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to form the STI to a desirable depth, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233 (1955).

9. As to claim 3: Yoshiko discloses **an insulation film covering the bottom and sidewalls of the isolation trench** (Figs. 2 and 5c; [0089]; insulation layer 5).

10. As to claim 11: Yoshiko fails to expressly disclose **a camera comprising the solid state imaging apparatus according to claim 1**. However, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to use the solid state imager as taught by Yoshiko and detailed in paragraph 8 in a camera as it is a well known technique in the art to use solid state devices as imaging apparatuses in cameras and the application of which is recognized to be within the ordinary capabilities of one skilled in the art and would have yielded the predictable results of a solid state imaging device with reduced dimension size ([0024]) and increased imaging capabilities. *KSR Int'l v. Teleflex Inc.*, 127 S. Ct., 1727 (2007).

11. As to claim 12: Yoshiko discloses **where the silicon material contains no impurities** ([0027]-[0030]; Yoshiko does not disclose doping the silicon material 7b with any impurities, hence the silicon material is implicitly free from the doping impurities).

12. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshiko as applied to claim 1 above, and further in view of Seo (US 2004/0048444 and Seo hereinafter).

As to claim 6: Yoshiko discloses **a MOS transistor formed in the imaging area** (Fig. 1; transistor 51 is in imaging area 37).

Yoshiko fails to expressly disclose

**where the isolation material contains an impurity of the opposite conductivity type to source and drain regions of the MOS transistor.**

In the same field of endeavor, Seo discloses **where the isolation material contains an impurity** (Abstract).

Given the teachings of Seo, a person having ordinary skill in the art at the time of the invention would have readily recognized the desirability and advantages of modifying Yoshiko by employing the well known or conventional features of STI manufacturing, such as displayed by Seo, by employing a doping step in an STI structure in order to form a porous silicon layer which results in an overall more efficient and design effective result ([0022]).

Yoshiko in view of Seo fail to expressly disclose where the impurity is **of the opposite conductivity type to source and drain regions of the MOS transistor**. However, the claim would have been obvious to a person having ordinary skill in the art at the time the invention was made since, as stated in KSR Int'l v. Teleflex Inc., 127 S. Ct., 1727 (2007), a person having ordinary skill in the art has good reason to pursue the known options within his or her technical field (in this case, the two generic types of impurity conductivity types, p or n); if this leads to the anticipated success (in the instant case, an isolation region with desired electrical properties), it is likely the product not of innovation but of ordinary skill and common sense.

13. As to claim 7: Yoshiko in view of Seo discloses **the isolation material is made of amorphous silicon, polycrystalline silicon or porous silicon** (Abstract; porous silicon). The claim would have been obvious to a person having ordinary skill in the art

at the time the invention was made since the technique of using porous silicon in an STI structure was a technique well known in the art and, in view of the teachings of Seo, recognized to be within the ordinary capabilities of one skilled in the art and would have yielded the predictable results of providing an STI with improved isolation and critical dimension capabilities ([0022]). KSR Int'l v. Teleflex Inc., 127 S. Ct., 1727 (2007).

14. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshiko in view of Williams et al (US 6,900,091 and Williams hereinafter).

Yoshiko discloses **a method for fabricating a CMOS (complementary-metal-oxide-semiconductor) solid state imaging apparatus having an N-channel type transistor, a P-channel type transistor, and a photoelectric conversion section** ([0016]; CMOS implicitly has an N-channel and P-channel type transistor), **said method comprising the steps of: forming an isolation trench (4) by etching a region of the silicon substrate (Fig. 5(b); [0088]); forming an insulating film (5) to cover the bottom and sidewalls of the isolation trench (Fig. 5(c); [0089]); after the formation of the insulating film, filling the isolation trench with a silicon layer (Fig. 6(e); [0092]; silicon layer 7a).**

Yoshiko fails to expressly disclose **implanting an impurity into a predetermined region of the silicon layer, wherein during the step of implanting an impurity, a P-type impurity is implanted into a region between the N-channel transistors in the isolation region, and a region between the N-channel transistor and the photoelectric conversion section in the isolation region, and wherein**



**during the step of implanting an impurity, an N-type impurity is implanted into a region between the P-channel transistors in the isolation region, and a region between the P-channel transistor and the photoelectric conversion section in the isolation region.**

In the same field of endeavor, Williams discloses **implanting an impurity into a predetermined region of the silicon layer, wherein during the step of implanting an impurity, a P-type impurity is implanted into a region between the N-channel transistors in the isolation region, and a region between the N-channel transistor and the photoelectric conversion section in the isolation region, and wherein during the step of implanting an impurity, an N-type impurity is implanted into a region between the P-channel transistors in the isolation region, and a region between the P-channel transistor and the photoelectric conversion section in the isolation region** (Abstract and col. 6, lines 59-67). Williams discloses a method by which photodiodes, P/N-channel resistors, etc. can be isolated from each other by doping using a desired impurity type (if dealing with a transistor, the opposite conductivity type of the transistor is used to provide isolation) between the devices and in the isolation region. Yoshiko also discloses implanting impurities in the isolation region 7b [0082], but such that it extends only so far. Therefore, given the teachings of Williams, a person having ordinary skill in the art at the time of the invention would have readily recognized the desirability and advantages of modifying Yoshiko by employing the well known or conventional features of semiconductor device isolation, such as

displayed by Williams, by employing impurity doping steps after formation of devices in order to provide improved isolation between different/adjacent semiconductor devices.

15. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshiko in view of Williams as applied to claim 8 above, and further in view of Lee (US 2004/0127035 and Lee hereinafter).

As to claim 9: Although the method disclosed by Yoshiko in view of Williams shows substantial features of the claimed invention (discussed in paragraph 14 above), it fails to expressly disclose:

**making the silicon layer porous.**

Nonetheless, this feature is well known in the art and would have been an obvious modification of the method disclosed by Yoshiko in view of Williams, as evidenced by Lee.

In the same field of endeavor, Lee discloses **making the silicon layer porous** ([0028]).

Given the teachings of Lee, a person having ordinary skill in the art at the time of the invention would have readily recognized the desirability and advantages of modifying Yoshiko in view of Williams by employing the well known or conventional features of STI manufacturing, such as displayed by Lee, by employing a step to make the substrate porous in order to provide a means for forming an STI structure which overcomes/obviates problems, such as critical dimension control, overhang, voids, etc. ([0007]), with conventional STI etching techniques.

16. As to claim 10: Yoshiko in view of Williams in view of Lee disclose **attaching an electrode to part of the silicon layer** (Fig. 1; [0011] and [0021]); **and immersing in a solution, part of the silicon layer excluding the part thereof to which the electrode is attached and then passing current via the electrode through the silicon layer** (Fig. 1; [0011] and [0021]; Examiner interprets that solution 160 (electrolyte) is formed only on the top surface of the wafer and does not occur in the area underneath the wafer, i.e., the area where the work electrode exists). Given the teachings of Lee, a person having ordinary skill in the art at the time of the invention would have readily recognized the desirability and advantages of modifying Yoshiko in view of Williams by employing the well known or conventional features of STI manufacturing, such as displayed by Lee, by employing a step to make the substrate porous in order to provide a means for forming an STI structure which overcomes/obviates problems, such as critical dimension control, overhang, voids, etc. ([0007]), with conventional STI etching techniques.

#### ***Response to Arguments***

17. Applicant's arguments with respect to claims 1, 3, and 6-12 have been considered but are moot in view of the new ground(s) of rejection.

#### ***Conclusion***

18. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph C. Nicely whose telephone number is (571) 270-3834. The examiner can normally be reached on Monday through Friday 7:30AM-5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Joseph C. Nicely/  
Examiner, Art Unit 2813

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